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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,068	03/19/2001	Laurence H. Cooke	262/043	9013

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LYON & LYON LLP
633 WEST FIFTH STREET
SUITE 4700
LOS ANGELES, CA 90071

EXAMINER
THOMPSON, ANNETTE M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,068	COOKE ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This application, 09/812,068, has been examined. Claims 2-23 are pending.

Information Disclosure Statement

1. Although the information disclosure statement filed 13 April 2001 complies with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609, some of the references are currently not considered because they cannot be found in the parent application. Examiner requested a duplicate of the references and Peter Mei, 39,768, responded via a voice mail message, on or around June 20, 2002, and informed that reference copies would be sent as soon as possible. Upon document receipt, Examiner will consider and sign off on the references listed on the PTO-1449. Examiner appreciates Applicants' efforts to facilitate the prosecution of the instant application.

Drawings

2. The drawings are objected to: At Figure 25, in the last decision box, correct spelling to constraint. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: At page 1, line 10, insert status of Application (e.g. *now patented,* etc.). At page 2, line 5, "manufactures" should be *manufacturers.* Page 85, line 1 (Using DFT rules) should have a header distinct from page 88, line 7, (using DFT rules). Appropriate correction is required.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it exceeds 300 words. Correction is required. See MPEP § 608.01(b).

Claim Objections

6. **Claims 2, 6, 7, 9, 11, 13, 17, 18, 20** are objected to based on the following reasoning: Pursuant to **claim 2**, at line 2, after "selecting" change "a" to *an*. Additionally, claim 2, step (e), performs verification of the derivative circuit block. However, the derivative circuit block was not formerly created/designed. Examiner suggests the addition or modification of an existing step to add or clarify derivative circuit block creation. **Claim 13** addresses the limitations objected to in claim 2. Therefore the claim 2 objections are applicable to claim 13. Pursuant to **claim 6**, at line 1, after "added" insert - -to - -. Pursuant to **claim 17**, at line 2, after "added" insert - -to - -. Pursuant to **claims 7 and 18**, at line 1, use common letters in referencing steps *a* and *e*. Pursuant to **claims 9 and 20**, after "chip" insert - -layout- -. Pursuant to claim 11, it appears that Applicants are trying to claim the features disclosed in Applicants'

specification at ¶ 120. For clarity, Examiner suggests either replacing the phrase "programmable fabrics each has a port access and hierarchical routing" with *programmable fabrics each have programming ports and are hierarchically routed* or inserting some other similarly accurate phraseology. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 3, 7, 9, 14, 18, 20** rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Pursuant to **claims 3 and 14**, the limitation of "altering the chip layout" presupposes an existing chip layout prior to planning the chip layout. This is contrary to common circuit design processes and furthermore is not disclosed in Applicants' specification. Therefore, Applicants must clarify these claims to enable accurate claim interpretation and examination. For examination purposes, these claims are interpreted to mean that *altering the chip layout does not result in altering the one or more programmable fabrics*. (see specification, page 84, lines 17-21) Pursuant to **claim 9** (at line 1), and **claim 20** (at line 2), "the chip" lacks antecedent basis. Pursuant to **claims 7 and 18**, the limitations recited would suggest that as a result of designing a second derivative design, the original circuit design used to create the second derivative design either is or becomes a derivative design. These claims are confusingly worded and it is not known what Applicants mean by this limitation. Furthermore, the specification does not clarify this limitation. For purposes of

examination, Examiner treats the claim as *the iteration of steps a through e to design a second derivative design.*

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of Claims 2-23

11. **Claims 2-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent 6,175,948 ("Miller") and the Herbert-Dawid et al. paper (Dawid paper") entitled ADPCM Codec: From System Level Description to versatile HDL Model. Miller discloses a methodology and apparatus for designing a waveform compiler, a Digital Signal Processor (DSP) type of model (see Miller, col. 5, ll. 50-57 and col. 6, ll. 10-13). Although one of ordinary skill in the art should recognize that a power analysis

would be part of a DSP design methodology, Miller does not explicitly disclose a power analysis step. The Dawid paper discloses a common DSP system design methodology and environment (see Dawid, page 459, Figure 1, which details the DSP design methodology) and explicitly discloses the necessary power analysis considerations. It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to use or reference the DSP design methodology disclosed in the Dawid paper for further detailed disclosure or information regarding the DSP design methodology used in Miller. In this Office Action, the cites reference the Miller '948 patent unless the Dawid paper is specifically indicated.

12. Pursuant to claim 2 which recites [a] method for designing a derivative circuit block (col. 5, ll. 41-44 discloses reuse programming as a primary goal and a derivative circuit block, as disclosed by Applicants, is a reusable circuit block) comprising selecting an original circuit design (the waveform compiler, col. 5, ll. 50-57), wherein the original circuit design comprises one or more programmable fabrics (new library building blocks, col. 5, ll. 58-62); performing front-end acceptance testing on the circuit design (col. 5, line 58 to col. 6, line 5); planning a chip layout (col. 6, ll. 6-10); programming at least one of the one or more programmable fabrics (col. 6, ll. 10-19) and performing verification of the derivative circuit block (col. 6, ll. 45-50).

13. Pursuant to claim 3, wherein the step of planning the chip layout does not result in altering the chip layout (col. 6, ll. 6-16).

14. Pursuant to claim 4, further comprising the step of performing clocking and timing analysis prior to the step of performing verification of the derivative circuit block (see Fig. 9, step 910; also col. 13, line 67 to col. 14, line 11.

15. Pursuant to claim 5, further comprising the step of performing power analysis prior to the step of performing verification of the derivative circuit block (*Dawid's* Figure 1 illustrates a power analysis (*Dawid's* "power consumption") prior to verification.

16. Pursuant to claim 6, wherein only a set of new functionality added to the original circuit design and any functionality interfacing with the set of new functionality is tested or verified (col. 7, line 64 to col. 8, line 9 suggests this limitation)

17. Pursuant to claim 7, wherein steps a through e are repeated to design a second derivative design: col. 17, line 55 to col. 18, line 27 suggest this limitation (e.g. "modules can be added" and "user library component creation".

18. Pursuant to claim 8, wherein the step of planning the chip layout comprises analyzing timing requirements (col. 4, ll. 24-30; see also col. 17, ll. 8-12) to ensure the derivative circuit block meets all applicable timing requirements.

19. Pursuant to claim 9, further comprising the step of assembling the chip layout col. 6, ll. 51-53 suggests this step of completion (i.e. "the design is ready for the target implementation).

20. Pursuant to claim 10, wherein the original circuit design further comprises one or more non-programmable fabrics (existing library building blocks, col. 5, ll. 58-62).

21. Pursuant to claim 11, wherein the one or more programmable fabrics each has a port access and hierarchical routing (col. 10, ll. 1-8 and ll. 15-27 disclose the use of

FPGAs which Applicants have disclosed (specification, page ¶ 120) as a programmable fabric with inherent programming access and hierarchical levels).

22. Pursuant to claim 12, further comprising the step of determining a power level for each programmable fabric and each non-programmable fabric through simulation (the *Dawid* paper, page 464, Figure 5 illustrates this limitation).

23. Pursuant to independent claim 13 and dependent claims 14-23, these claims respectively address the method limitations already considered and rejected in independent claim 2 and dependent claims 3-12, respectively and additionally recites a computer readable medium for executing the claimed method. The use of database systems as disclosed by Miller (col. 15, ll. 47-67) and the Dawid paper for implementing a DSP design methodology necessarily includes the use of computer readable media. Therefore, claims 13-23 are likewise rejected based on the rationale outlined in claims 2-12, supra.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please reference the PTO-892 for a complete listing.

- Baxter, U.S. Patent 5,815,405, discloses a method and apparatus for converting a programmable logic device representation of a circuit into a second representation of a circuit.
- Payne, U.S. Patent 6,338,158, discloses custom hardware IC modeling using standard ICS for use in IC design validation.

25. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703)306-3329.

26. Responses to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)
(703)872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).

A. M. THOMPSON
Patent Examiner

June 27, 2002